CLAIMS

What is claimed is:

1. A circuit, comprising:
   a) a differential signal transmission line;
   b) a common mode circuit in communication with said differential signal transmission line, configured to reduce a swing of said differential signal transmission line; and
   c) at least one overvoltage protection circuit in communication with said common mode circuit, wherein at least part of said common mode circuit is electrically interposed between said overvoltage protection circuit and said differential signal transmission line.

2. The circuit of Claim 1, wherein said common mode circuit comprises first and second resistors in series.

3. The circuit of Claim 2, wherein said overvoltage protection circuit is coupled to a node between said first and second resistors.

4. The circuit of Claim 2, wherein said first and second resistors comprise first and second termination resistors.

5. The circuit of Claim 2, further comprising an input buffer configured to receive a differential signal from said differential signal transmission line.

6. The circuit of Claim 5, wherein said first and second resistors each have a resistance less than a resistance component of an impedance of said input buffer.

7. The circuit of Claim 2, wherein said common mode circuit further comprises a third resistor configured to receive a common mode voltage.

8. The circuit of Claim 7, wherein said third resistor is coupled to a node between said first and second resistors.

9. The circuit of Claim 8, wherein said overvoltage protection circuit is also coupled to said node between said first and second resistors.

10. The circuit of Claim 8, wherein said third resistor has a resistance at least ten times greater than a resistance of said first and second resistors.

11. The circuit of Claim 10, wherein said third resistor has a resistance at least one hundred times greater than said resistance of said first and second resistors.

12. The circuit of Claim 1, further comprising first and second input terminals configured to receive a differential signal for said differential signal transmission line.

13. The circuit of Claim 1, wherein said differential signal transmission line comprises a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit.

14. The circuit of Claim 13, wherein said common mode circuit comprises first and second resistors in series between said first and second conduits, and said overvoltage protection circuit is coupled to a node between said first and second resistors.

15. The circuit of Claim 1, wherein said differential signal transmission line has a maximum voltage swing of less than 2 volts.

16. The circuit of Claim 1, wherein said differential signal transmission line has a maximum voltage swing of less than 1.5 volts.

17. The circuit of Claim 1, wherein said at least one overvoltage protection circuit comprises at least one diode.

18. The circuit of Claim 17, wherein said at least one diode has a threshold voltage greater than a voltage swing of said differential signal transmission line.

19. The circuit of Claim 17, wherein said at least one overvoltage protection circuit comprises at least two diodes in series.

20. The circuit of Claim 1, wherein said at least one overvoltage protection circuit is in further communication with a low impedance node.

21. The circuit of Claim 20, wherein said low impedance node comprises a power supply node, a virtual ground node or a ground potential.

22. The circuit of Claim 4, wherein said common mode circuit further comprises third and fourth resistors in series between said first and second termination resistors.

23. The circuit of Claim 22, wherein said at least one overvoltage protection circuit comprises (i) a first overvoltage protection circuit coupled to a first node between said first termination resistor and said third resistor, and (ii) a second overvoltage protection circuit coupled to a second node between said second termination resistor and said fourth resistor.

24. A circuit, comprising:
    a) means for transferring a differential signal;
    b) means for reducing a swing of said means for transferring; and
    c) at least one means for protecting circuitry to which said differential signal is to be transferred from an overvoltage, wherein at least part of said means for reducing is electrically interposed between said at least one means for protecting and said means for transferring.

25. The circuit of Claim 24, wherein said means for reducing comprises first and second resistors in series.

26. The circuit of Claim 25, wherein said at least one means for protecting is coupled to a node between said first and second resistors.

27. The circuit of Claim 25, further comprising a means for buffering said differential signal, configured to receive said differential signal from said means for transferring.

28. The circuit of Claim 27, wherein said first and second resistors each have a resistance less than a resistance component of an impedance of said means for buffering.

29. The circuit of Claim 24, wherein said means for reducing comprises a means for applying a common mode voltage.

30. The circuit of Claim 29, wherein said means for applying is coupled to a node between first and second means for terminating said differential signal.

31. The circuit of Claim 29, wherein said means for applying a common mode voltage comprises a resistor receiving said common mode voltage.

32. The circuit of Claim 31, wherein said resistor has a resistance at least one hundred times greater than said resistance of said first and second means for terminating.

33. The circuit of Claim 32, wherein said at least one means for protecting is also coupled to said node between said first and second means for terminating.

34. The circuit of Claim 24, wherein said means for transferring comprises a differential signal transmission line.

35. The circuit of Claim 34, further comprising means for receiving said differential signal for said differential signal transmission line.

36. The circuit of Claim 34, wherein said differential signal transmission line comprises a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit.

37. The circuit of Claim 36, wherein said means for reducing comprises first and second resistors in series between said first and second conduits, and said at least one means for protecting is coupled to a node between said first and second resistors.

38. The circuit of Claim 24, wherein said means for transferring has a maximum voltage swing of less than 2 volts.

39. The circuit of Claim 24, wherein said at least one means for protecting comprises at least one diode.

40. The circuit of Claim 39, wherein said at least one diode has a threshold voltage greater than a voltage swing of said means for transferring.

41. The circuit of Claim 26, wherein said at least one means for protecting is in further communication with a low impedance node.

42. The circuit of Claim 25, wherein said means for reducing further comprises third and fourth resistors in series between said first and second resistors.

43. The circuit of Claim 42, wherein said at least one means for protecting comprises (i) a first means for protecting coupled to a first node between said first and third resistors, and (ii) a second means for protecting coupled to a second node between said second and fourth resistors.

44. An integrated circuit, comprising:
    a) first and second input terminals configured to receive a differential signal;
    b) an input buffer configured to receive said differential signal; and
    c) the circuit of Claim 1, wherein said differential signal transmission line communicates said differential signal from said input terminals to said input buffer.

45. The integrated circuit of Claim 44, wherein said common mode circuit comprises first and second resistors in series.

46. The integrated circuit of Claim 45, wherein said at least one overvoltage protection circuit is coupled to a node between said first and second resistors.

47. The integrated circuit of Claim 45, wherein said first and second resistors each have a resistance less than a resistance component of an impedance of said input buffer.

48. The integrated circuit of Claim 45, wherein said common mode circuit further comprises a third resistor configured to receive a common mode voltage.

49. The integrated circuit of Claim 48, wherein said third resistor is coupled to a node between said first and second resistors.

50. The integrated circuit of Claim 48, wherein said third resistor has a resistance at least one hundred times greater than said resistance of said first and second resistors.

51. The integrated circuit of Claim 44, wherein said differential signal transmission line comprises a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit.

52. The integrated circuit of Claim 51, wherein said common mode circuit comprises first and second resistors in series between said first and second conduits, and said at least one overvoltage protection circuit is coupled to a node between said first and second resistors.

53. The integrated circuit of Claim 44, wherein said differential signal transmission line has a maximum voltage swing of less than 2 volts.

54. The integrated circuit of Claim 44, wherein said at least one overvoltage protection circuit comprises at least one diode.

55. The integrated circuit of Claim 54, wherein said at least one diode has a threshold voltage greater than a voltage swing of said differential signal transmission line.

56. The integrated circuit of Claim 44, further comprising first and second input pins respectively coupled to said first and second input terminals and configured to receive an external differential signal.

57. The integrated circuit of Claim 44, wherein said at least one overvoltage protection circuit is in further communication with a low impedance node.

58. The integrated circuit of Claim 57, wherein said low impedance node comprises a power supply node, a virtual ground node or a ground potential.

59. The integrated circuit of Claim 52, wherein said common mode circuit further comprises third and fourth resistors in series between said first and second resistors.

60. The integrated circuit of Claim 59, wherein said at least one overvoltage protection circuit comprises (i) a first overvoltage protection circuit coupled to a first node between said first and third resistors, and (ii) a second overvoltage protection circuit coupled to a second node between said second and fourth resistors.

61. A system for transferring data on or across a network, comprising:
    a) the integrated circuit of Claim 44;
    b) at least one transmitter communicatively coupled to said first and second input terminals, said transmitter being configured to transmit a differential data signal; and
    c) at least one receiver communicatively coupled to said input buffer, said receiver being configured to receive said differential data signal.

62. The system of Claim 61, wherein said integrated circuit further comprises said receiver.

63. A network, comprising:

a) a plurality of the systems of Claim 61, communicatively coupled to each other; and

b) a plurality of storage or communications devices, each of said storage or communications devices being communicatively coupled to one of said systems.

64. The network of Claim 63, wherein each of said storage or communications devices comprises a storage device.

65. An integrated circuit, comprising:

a) means for receiving a differential signal;

b) means for buffering said differential signal; and

c) the circuit of Claim 24, wherein said means for transferring communicates said differential signal from said means for receiving to said means for buffering.

66. The integrated circuit of Claim 65, wherein said means for reducing comprises first and second means for terminating said differential signal.

67. The integrated circuit of Claim 66, wherein said at least one means for protecting is coupled to a node between said first and second means for terminating.

68. The integrated circuit of Claim 66, wherein said first and second means for terminating each comprise a resistor having a resistance less than a resistance component of an impedance of said means for buffering.

69. The integrated circuit of Claim 66, wherein said means for reducing comprises a resistor configured to receive a common mode voltage.

70. The integrated circuit of Claim 69, wherein said resistor is coupled to a node between said first and second means for terminating.

71. The integrated circuit of Claim 70, wherein said at least one means for protecting is also coupled to said node between said first and second means for terminating.

72. The integrated circuit of Claim 70, wherein said resistor has a resistance at least one hundred times greater than a resistance of said first and second means for terminating.

73. The integrated circuit of Claim 65, wherein said means for transferring comprises a first conduit and a second conduit, wherein said second conduit is complementary to said first conduit.

74. The integrated circuit of Claim 73, wherein said means for reducing comprises first and second means for terminating in series between said first and second conduits, and said at least one means for protecting is coupled to a node between said first and second resistors.

75. The integrated circuit of Claim 65, wherein means for transferring has a maximum voltage swing of less than 2 volts.

76. The integrated circuit of Claim 65, wherein said at least one means for protecting comprises at least one diode.

77. The integrated circuit of Claim 76, wherein said at least one diode has a threshold voltage greater than a voltage swing of said means for transferring.

78. The integrated circuit of Claim 65, further comprising means for receiving an external differential signal coupled to said means for transferring.

79. The integrated circuit of Claim 65, wherein said at least one means for protecting is in communication with a low impedance node.

80. The integrated circuit of Claim 67, wherein said means for reducing further comprises first and second resistors in series between said first and second means for terminating.

81. The integrated circuit of Claim 80, wherein said at least one means for protecting comprises (i) a first means for protecting coupled to a first node between said first means for terminating and said first resistor, and (ii) a second means for protecting coupled to a second node between said second means for terminating and said second resistor.

82. A system for transferring data on or across a network, comprising:
    a) the integrated circuit of Claim 65;
    b) at least one means for transmitting a differential data signal, communicatively coupled to said means for transferring; and
    c) at least one means for receiving said differential data signal, communicatively coupled to said means for buffering.

83. The system of Claim 82, wherein said integrated circuit further comprises said means for receiving.

84. A network, comprising:
    a) a plurality of the systems of Claim 82, communicatively coupled to each other; and

b) a plurality of means for storing or communicating, each of said means for storing or communicating being communicatively coupled to one of said systems.

85. The network of Claim 84, wherein each of said means for storing or communicating comprises a means for storing.

86. A method of protecting a differential circuit from an overvoltage, comprising the steps of:

a) receiving a differential signal in said differential circuit;

b) controlling a voltage swing of said differential signal with a termination circuit in communication with said differential circuit; and

c) when said differential circuit receives said overvoltage, shunting said overvoltage to a low impedance node through said termination circuit, and otherwise, processing said differential signal through circuitry coupled to said differential circuit.

87. The method of Claim 86, wherein said shunting comprises passing said overvoltage through at least one diode.

88. The method of Claim 86, wherein said low impedance node comprises a power supply node, a virtual ground node or a ground potential.

89. The method of Claim 86, wherein said shunting comprises passing said overvoltage through at least one diode.

90. The method of Claim 86, wherein said termination circuit comprises first and second resistors having a common mode node therebetween.

91. The method of Claim 90, wherein said controlling step comprises applying a common mode voltage to said common mode node.

92. The method of Claim 91, wherein said common mode voltage is applied to said common mode node through a resistor having a resistance greater than a resistance component of an impedance of said circuitry.

93. The method of Claim 92, further comprising the step of generating said common mode voltage.

94. The method of Claim 86, wherein said processing comprises buffering said differential signal.

95. The method of Claim 86, wherein said differential circuit comprises (i) first and second input pads and (ii) a differential signal transmission line electrically coupled to said first and second input pads.

96. The method of Claim 95, wherein said termination circuit comprises a first resistor coupled to a first conduit of said differential signal transmission line, a second resistor coupled to a second conduit of said differential signal transmission line, and a common mode node between said first and second resistors, wherein said second conduit is complementary to said first conduit.